EZoFlash, Willem programmer. Info for SW developer. v0.1 09.08.2010

Schematic source:
EZoFlash4v4 - http://www.ezoflash.com/downloads/ezoflash4v4_sch.pdf
EZoFlash4v5 - http://www.ezoflash.com/downloads/ezoflash4v5_sch.gif
pcb3b - http://www.ezoflash.com/willem/pcb3b_sch.pdf
pcb45 - http://www.ezoflash.com/willem/pcb45c_sch_by_EZo.pdf

Driver: io.dll
Parallel port : LPT1 by default. Apply command to edit/assign new port adress.

Port signals:

Data port : Outputs.

Data 0 – pin2 – DO0
1) parallel memory data bit 0 (D0)
2) parallel memory adress load clock (4015/C)
3) serial memory data out
4) test hardware controlsignal

Data 1 – pin3 – DO1
1) parallel memory data bit 1 (D1)
2) parallel memory adress load serial data (first 4015/D)

serial data A23..A0 in pcb3b mode, serial data A7..A0 in pcb45 mode
3) parallel memory chip output data latch in output register (4014/4021/pin9 P/S) , set output register in serial mode
4) serial memory clock out (D1/RB6)

Data 2 – pin4 – DO2
1) parallel memory data bit 2 (D2)
2) paralel memory output register clock , inverted (4014/4021 pin10 CLK)

Data 3 – pin5 – DO3
1) parallel memory data bit 3 (D3)

Data 4 – pin6 – DO4
1) parallel memory data bit 4 (D4)
2) parallel memory adress load serial data (4015/D) , serial adress data A15..A8 , only pcb45 mode

Data 5 – pin7 – DO5
1) parallel memory data bit 5 (D5)
2) parallel memory adress load serial data (4015/D) , serial adress data A23..A16 , only pcb45 mode

Data 6 – pin8 – DO6
1) parallel memory data bit 6 (D6)

Data 7 – pin9 – DO7
1) parallel memory data bit 7 (D7)

Status port : Inputs

Bit0
Bit1
Bit2
Bit3

Bit4 Select – pin13 (SELECT)
1) parallel memory data bit serial read (4021/Q6 pin2+invertor) , only pcb45 mode

Bit5 Paper Out – pin12 (PAPER END)
1) parallel memory data bit serial read (4021/Q7 pin12+invertor) , only pcb45 mode

Bit6 ACK – pin10 (ACK)
1) parallel memory data byte serial read (4021/Q6 pin2+invertor) , pcb35 mode
2) parallel memory data bit serial read (4021/Q6 pin2+invertor) , pcb45 mode

Bit7 Busy – pin11 (BUSY)
1) serial memory data read
2) test hardware controlsignal read

Control port :

Bit0 Strobe – pin1 (STB)

1) Vpp ON / Vpp OFF (bit log1/log0).

Bit1 Auto Linefeed – pin14 (AUTO)

1) Parallel memory signal OE# (S6/OE),

- bit log1 enable parallel memory chip output (invertor, OE#-log0)
- bit log0 enable parallel memory chip data input (invertor, OE# -log1)

2) Parallel port buffer data selection ;

both chips 4503 D1-D4 /E1# and D5-D6/E2# for willem/ezoflash4v4,
74HC244/E1#/E2# and 4503/E1 for ezoflash4v5

- bit log0 enable 4503 D1-D4/Q1-Q4 (data DO0-DO3 > D0-D3, DO4-DO7 > D4-D7) to parallel memory chip inputs ; both 4503/pin1 E1# log0 (willem/ezoflash4v4),
- bit log0 enable 74HC244 D0-D7/Q0-Q7 (data DO0-DO7 > D0-D7) to parallel memory chip inputs ; 74HC244 pins1/19 E1#/E2# log0 (ezoflash4v5)
- bit log1 enable 4503 D5-D6/Q5-Q6, clock (DO0 > CLK) and adress data (DO1 > D) to adress register (4015) for willem / ezoflash4v4.

Note, in pcb45 mode only adress data A0..A7 are buffered.

- bit log1 enable 4503 D1-D4/Q1-Q4, clock (DO0 > CLK) and adress data (DO1, DO4, DO5) to adress register (4015) for ezoflash4v5

3) Parallel memory output register data latch/mode enable

- bit log1 enable first 4503 D5/Q5 (for willem/ezoflash4v4), 4503 D2/Q2 (for ezoflash4v5)

Bit2 Init – pin16 (INIT)

1) Vcc ON / Vcc OFF (bit log1/log0).

Bit3 Select Printer – pin17 (SELIN)

1) Parallel memory signal WE (S4/WE/CE)
2) Serial memory 24Cxxx pin7 WP#, bit log1 to enable write
3) Serial memory 93Cxxx pin1 CS, bit log0 to enable chip
4) Serial memory 25Cxxx pin1 CS#, bit log0 to enable chip
5) SPI Flash 25xxxx pin1 CS#, Reset and Chip Select, bit log0 to enable chip

Bit4
Bit5
Bit6
Bit7

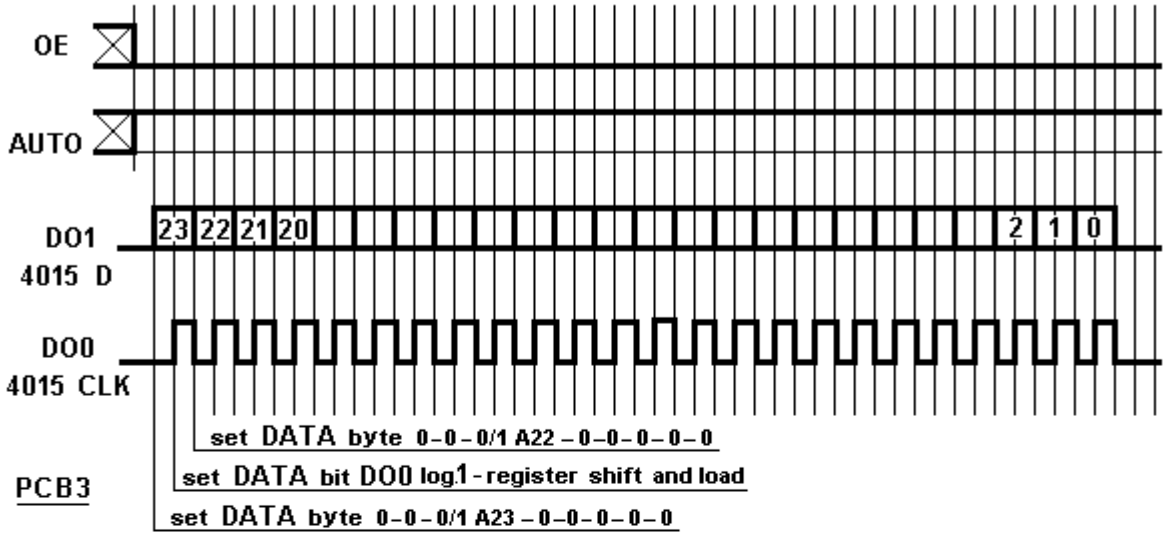
Hardware level commands

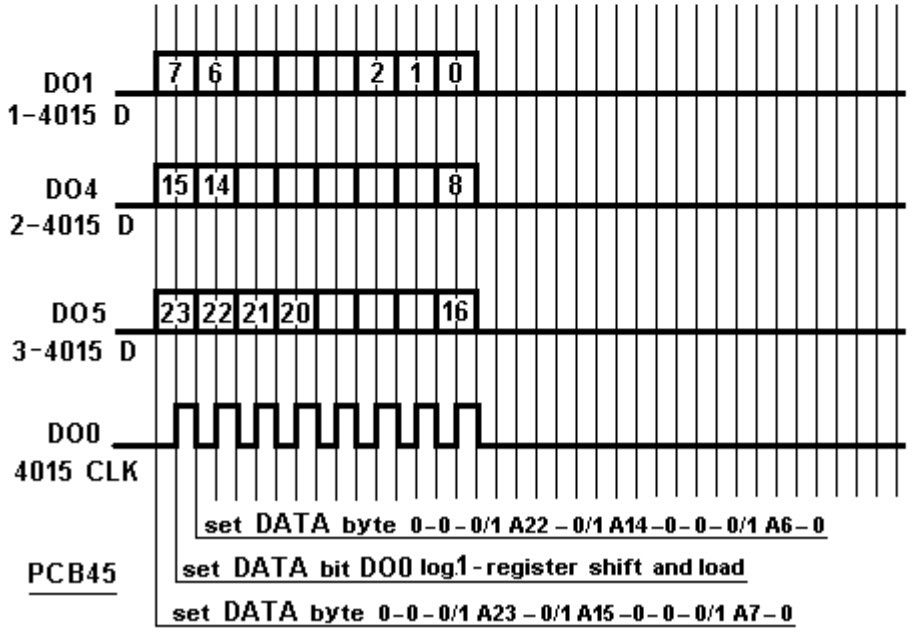
1. VCC_ON, VCC_ OFF . Port signal INIT levels log0/log1
2. VPP_ON, VPP_OFF . Port signal STB levels log0/log1
3. OE_LOW, OE_HIGH. Port signal AUTO inverted levels log1/log0.
4. WE_LOW, WE_HIGH. Port signal SELIN levels log0/log1.
5. READ_SERBIT. Read port signal BUSY.
6. **PRG_RST**
   Command reset all signals in correct sequence. Required after SW launch, exit command .
   - VPP OFF
   - VCC OFF
   - WRITE_ADRESS (0x000000) (optional)
   - OE_LOW
   - WE_LOW
   - Set DO0…DO7 (0x00)
7. **HW_CHECK**
   Command check pulse throughput from DO0 to BUSY.
   - PRG_RST
   - VCC_ON
   - OE_HIGH
   - Set bit DO0_HIGH
   - DELAY (2) (delay in microseconds, to be defined)
   - READ_SERBIT. If log.1 – PASS, if log.0 – Hardware error.
   - Set bit DO0_LOW
   - DELAY (2) .
   - READ_SERBIT. If log.0 – PASS, if log.1 – Hardware error.
   - PRG_RST.

   Hardware failures
   a) not connected programmer;
   b) not powered programmer;
   c) wrong parallel port adress , not able set signals;
   d) Vcc failure (overload – significant Vcc drop , voltage switch failure,..)

   Execute HW_CHECK in any chip operation command (Write,Read,GetID,Verify,…) after VCC_ON. In case of voltage drop due to wrong placed chip operations with HW and chip are terminated.
   HW_CHECK PASS identify connected willem compatible programmer.
8. **PRG_ID**
   Command similar to HW_CHECK, allow identify willem/ezoflash programmer type.
   EZoFlash feature – pulse from DO0 to BUSY set up is faster , less delay (in willem pulse pass 2 transistors and 2 logic elements, in ezoflash4v4 – 1 transistor and 1 logic element, in ezoflash4v5 – 4 logic elements). No delay or less than 1mks in HW_CHECK ezoflash4v4/4v5 PASS, willem programmers FAIL. Next HW_CHECK with OE_LOW allow identify 4v4 (PASS) or 4v5 (FAIL).
   Here are ideas to identify pcb3b or pcb45 compatible programmers.
   More details can be provided.

9. SET_ADRESS (0x000000) - A23..A0 in HEX





10. READ_PARBYTE